
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Aronowitz et al.

Attorney Docket No.:
02-6037/LSIIP218

Application No.: Not yet assigned

Examiner: Not yet assigned

Filed: Herewith

Group: Not yet assigned

Title: MEMORY DEVICE HAVING AN
ELECTRON TRAPPING LAYER IN A HIGH-K
DIELECTRIC GATE STACK

INFORMATION DISCLOSURE STATEMENT
37 CFR §§1.56 AND 1.97(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

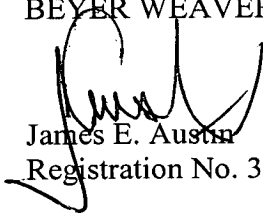
Dear Sir:

The references listed in the attached PTO Form 1449, copies of which are attached, may be material to examination of the above-identified patent application. Applicants submit these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is: (i) filed within three (3) months of the filing date of the above-referenced application, (ii) believed to be filed before the mailing date of a first Office Action on the merits, or (iii) believed to be filed before the mailing of a first Office Action after the filing of a Request for Continued Examination under §1.114. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 12-2252 (Order No. 02-6037).

Respectfully submitted,
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Form 1449 (Modified) Information Disclosure Statement By Applicant (Use Several Sheets if Necessary)	Atty Docket No.	Application No.:
	02-6037/LSI1P218	Not yet assigned
	Applicant:	
	Aronowitz et al.	
	Filing Date	Group
	Herewith	Not yet assigned

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	A	U.S. Patent Application Serial No. 10/123,263, filed April 15, 2002
	B	S. M. Sze, Physics of Semiconductor Devices (John Wiley & Sons, New York Ed., 1985) Section 8.6.2
	C	Guha et al., "Compatibility Challenges for High-K Materials Integration into CMOS Technology", MRS Bulletin, March 2002, p. 226-229
Examiner		Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.